REMARKS

As a preliminary matter, Applicant traverses the outstanding Office Action in its entirety. The newly cited references in the outstanding Office Action are not any more relevant to the present invention than the previously cited references that have been withdrawn by the Examiner. Applicant also takes particular exception to the unreasonable delay on the part of the Patent Office in acting on this case. The Office Action indicates that it is in response to the Appeal Brief filed on April 11, 2005, and no explanation has been given for the sixteen-month delay in responding.

Claims 2-3, 6, and 8-10 stand rejected under 35 U.S.C. 102(e) as being unpatentable over Bitzakidis et al. (U.S. 5,912,651). Applicant respectfully traverses this rejection in its entirety because a *prima facie* case of anticipation still has not been established against any of the present pending claims. The cited reference fails to teach most of the features of independent claim 2 of the present invention, and the reference even contradicts many of the Examiner's assertions about the reference.

For example, the Examiner erroneously asserts that the shift register/sample and hold circuits included in Bitzakidis' column driver circuit 22 (Fig. 1) somehow store display control information that is different from image data. Bitzakidis though, directly contradicts this assertion. Bitzakidis specifically teaches that "video data, (picture information), signals are supplied to the column conductors 16 from a column driver circuit 22 comprising one or more shift register/sample and hold circuits." (Col. 7, lines 39-42,

emphasis added). Bitzakidis even further states that "the circuit 22 is supplied with video data signals from a video processing circuit 24 and derived from the video signal applied to the input 25." (Col. 7, lines 42-45, emphasis added). In other words, even if the Examiner were correct that the sample and hold circuits in Bitzakidis' column driver circuit 22 could be reasonably interpreted to be memories, Bitzakidis unambiguously teaches that the only data supplied to such circuits is image (video) data. The Examiner has thus clearly misread the reference, and the rejection must be withdrawn for at least these reasons.

The rejection of claim 2 is also deficient on its face because the rejection improperly relies upon an unsupported theory of inherency. On page 5, lines 4-5 of the outstanding Office Action, the Examiner asserts that Bitzakidis' shift register "inherently *can be* used to store information to control the row driver circuit." (Emphasis added). This statement, however, is self-contradictory. Inherency cannot be established by possibilities or probabilities. Even if the Examiner were correct that the shift register "can be" used in such a way (which Applicant does not concede), inherency is only established where the element actually is affirmatively described as being used as asserted. Bitzakidis, however, provides no such teachings (or suggestions), and the Examiner's assertion of inherency is therefore deficient on its face. Bitzakidis even specifically teaches that "the circuits 20, 21, 22, 24 and 26 are of generally conventional form," and therefore, one skilled in the art would not understand them to store display control information. (Col. 7, lines 51-52). Accordingly, for at least these additional reasons, the outstanding rejection must be withdrawn.

The rejection of independent claim 2 must still further be withdrawn because Bitzakidis fails to teach (or even suggest) many other of the recited features of the present invention. For example, nowhere does Bitzakidis teach that its circuits 20-22 control the display unit by display control information stored in the memories. The Examiner seems to be asserting that timing information is first stored in the sample and hold circuits, and then must be somehow equivalent to the stored display control information of the present invention. Bitzakidis though, specifically contradicts any such interpretation. As discussed above, Bitzakidis only teaches that *image data* is passed through the sample and hold circuits. Bitzakidis further teaches that the timing information discussed by the Examiner comprises only "regular timing pulses" (col. 7, lines 34-35) which, as clearly shown in Figs. 3-4 of the reference, are simple square pulses that one skilled in the art would not expect to be *stored* in a memory, and in such a "conventional" circuit. Accordingly, the rejection should be withdrawn for still these further reasons.

Lastly, the Examiner's additional assertions regarding the other features of claim 2 are also without merit. With respect to the recited data bus and address bus of claim 2, the Examiner appears to have once again failed to even consider these features of the claim. The Examiner only asserts that Bitzakidis shows two buses that are "exterior to the display *panel* 10." (Page 4 of the outstanding Office Action, second and third full paragraphs, emphasis added). Claim 2 of the present invention though, clearly recites that both the data bus and the address bus connect the recited memories to the exterior of the

display device, and not the display *panel*, which is also featured in the claim (as a "display unit"), but does not comprise the device as a whole.

The "buses" the Examiner cites from Bitzakidis cannot even be reasonably interpreted as analogous to a data bus and address bus of the present invention. The connection between Bitzakidis' video processing circuit 24 and the shift register 22 is described to contain only "video data signals" (col. 7, line 43), and not display control information. Bitzakidis does not teach (or suggest) that the line connecting the timing and control circuit 21 to the row driver circuit 20 contains any address signals. In fact, Bitzakidis specifically contradicts the Examiner's assertion in this regard. Bitzakidis expressly states that the row driver circuit 20 is "controlled by regular timing pulses from a timing and control circuit 21," and not address signals, as erroneously asserted. (Col 7, lines 32-34). The rejection is therefore deficient for at least these reasons as well, and must be withdrawn.

With respect to claim 6 of the present invention specifically, the rejection is even further deficient. Nowhere does Bitzakidis teach (or even suggest) that the column driver circuit 22 or the data processing circuit 24 ever store pattern data in the memories in addition to the display control information. Applicant even notes that the Examiner does not cite to any specific teaching or suggestion within the reference that supports this erroneous assertion. "Pattern data" is clearly defined in the present Specification, and nothing cited by the Examiner from Bitzakidis even remotely reads upon these features of the present invention.

The rejection of claim 8 of the present invention is also deficient on its face for similar reasons. Nowhere does Bitzakidis teach (or even suggest) that the light source 19, or any of the other circuits cited by the Examiner as relevant to claim 8, operate as a "display information acquisition circuit," as clearly defined in claim 8 of the present invention. Contrary to the Examiner's assertions, Bitzakidis never teaches that any of its circuits acquire information about the display unit. Applicant further notes that the Examiner does not cite to any particular teaching or suggestion from the reference that even supports this assertion. This rejection must therefore also be withdrawn.

The rejection of claims 9 and 10 is equally flawed. As discussed above, Bitzakidis does not even teach (or suggest) anything analogous to the present display information acquisition circuit. Bitzakidis though, even further fails to teach that any such circuits check the display unit, and that such checks are in order to acquire information regarding a defect of the display unit (claim 9) or information regarding coordinates of a position at which input is entered on the display unit (claim 10). Applicant notes that the Examiner's comments do not even discuss these particular features of these two claims. The Examiner underlines the phrase "display information" frequently, but never even discusses anything relating to a defect of the display unit, or position coordinates input to the display unit. Given that case has been subject to prosecution for over seven years, if the Examiner is not willing to consider all of the actual language recited in the claims, the Examiner should either allow the case, or reassign it to another Examiner.

Claims 4-5 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Bitzakidis in view of Sato et al. (U.S. 5,712,652). Applicant respectfully traverses this rejection for at least the reasons discussed above. Claims 4 and 5 depend directly or indirectly from independent claim 2. Accordingly, the rejection is deficient on its face for failing to teach or suggest each and ever feature and limitation of the claims, as required by Section 2143.03 of the MPEP.

The rejection of claims 4-5 is further deficient on its face because the Examiner has not cited to anywhere from either prior art reference that teaches or suggests the desirability of making the combination as proposed by the Examiner. The portion cited by the Examiner (col. 6, lines 15-19 of Sato) gives no motivation to combine the reference with anything from Bitzakidis, and merely states that an object of Sato's invention is to create a display device "simple in structure," "high in the display density," and "suitable for the...note book type personal computer." Nowhere does this broad statement of a general objective teach or suggest the desirability of making the combination proposed by the Examiner.

Sato merely states an objective of having a simple device with high display density, suitable for notebook computers. The actual proposed combination, however, is the circuit from Fig. 14 of Sato with the very different circuit from Fig. 1 of Bitzakidis. The single objective from Sato, as cited by the Examiner, hardly teaches the desirability of combining these two particular circuits. First, the Examiner has not even demonstrative how

these two circuits *can* even be combined. Second, and more importantly, the Examiner has not cited to any teaching or suggestion from either reference that says these two specific circuits should be combined. Section 2143.01 of the MPEP requires that the Examiner be able to point to such a teaching or suggestion from the references, or else obviousness cannot be established based on the proposed combination. In the present case, this requirement simply has not been met, and the proposed combination fails on its face.

Claim 11 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Bitzakidis in view of Ogishima (U.S. 5,818,558). Applicant respectfully traverses this rejection for at least the reasons discussed above. Claim 11 depends directly from independent claim 2, and Applicant has described in detail how Bitzakidis fails to teach or suggest a great many of the features and limitations of claim 2.

The rejection of claim 11 is also deficient for similar reasons to those discussed above with respect to claims 4-5. The Examiner has not cited to anywhere in either prior art reference that teaches or suggests the desirability of this combination, as also proposed by the Examiner. Once again, the Examiner asserts that a single statement from one of the two references regarding a broad objective to provide a high quality display, by itself, justifies the combination of such a reference with any other reference seeking a high quality display, which is essentially any other reference that includes a display. Nowhere, however, does the Examiner cite to any teachings or suggestions from the references that indicate the

desirability of combining together the particular elements the Examiner claims to be obvious. Accordingly, the rejection of claim 11 also fails for at least these additional reasons.

Even though all of the arguments discussed above clearly establish that no further amendments to the present claims are necessary, Applicant nonetheless has amended independent claim 2 herein yet one more time for grammatical clarity, and solely for the purpose of expediting prosecution. The Examiner can see that claim 2 now emphasizes a feature of the claims that should have already been understood, namely, that the data bus and the address bus of the present invention connect to each one of the novel memories of the present invention. The Examiner should have no difficulty understanding now that the two recited buses of the present claims connect each of the memories to the exterior of the display device, and also that none of the cited references now of record can read upon at least these features of the present invention, as well as all of the other novel features discussed above.

Accordingly, there should be no further reason for any delay in the Examiner allowing this case, once all of the claim language of all of the claims is given full consideration in light of the presently cited prior art. If the Examiner is still not willing to allow the case at this time, Applicant formally requests that either the case be reassigned to a different Examiner, or that the Examiner telephone Applicant's representative at the number below to arrange a time when both the Examiner and his and his present Supervisor are available to discuss all of the substantive issues of the case, as well as the examination history itself.

Respectfully submitted,

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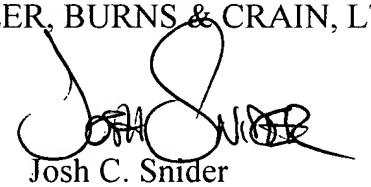
By 

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